CH32V103 Datasheet

V1.2

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Overview

Qingke 32-bit microprocessor RISC-V3A is based on RISC-V open-source instruction set design, and its system architecture achieves the best balance of low-cost, low-power consumption and functional applications of the hardware platform.

CH32V103 series general-purpose microcontrollers are equipped with a wealth of peripheral interfaces and functional modules, including clock security mechanism, multi-level power management, general DMA controller, multi-channel 12-bit ADC, multi-channel touch-key capacitance detection, advanced-control/general-purpose timers, USB2.0 host controller and device controller, multi-channel I2C/USART/SPI, etc. The microcontroller is equipped with a complete software and hardware platform and debugging interface tools, which can meet the needs of industrial, medical, consumer and other markets.

Features

- **Core:**

- RV32IMAC instruction set combination, hardware multiplication and division
- Fast programmable interrupt controller + Hardware on-site preservation and recovery
- Static branch prediction
- Conflict handling mechanism
- Up to 80MHz system frequency

- **Memory:**

- 20KB volatile data storage area, SRAM
- 64KB user application storage area, CodeFlash
- 3.75KB system storage area, BootLoader
- 128B system non-volatile configuration information memory area
- 128B user-defined information storage area

- **Power Management and Low Power:**

- Power supply range: 2.7V~5.5V, GPIO synchronous power supply voltage
- Low-power modes: Sleep/Stop/Standby
- V_{BAT} supply for RTC and backup registers independently

- **System clock and reset:**

- Built-in factory-trimmed 8MHz RC oscillator
- Built-in 40KHz RC oscillator
- Built-in PLL, optional CPU clock up to 80MHz
- External 4~16MHz high-speed oscillator
- External 32.768KHz low-speed oscillator
- Power-on/power-down reset (POR/PDR), programmable voltage detector (PVD)

- **Real-time clock (RTC): 32-bit independent timer**

- **General-purpose DMA controller:**

- Provide 7 channels
- Support peripheral and memory, memory and memory
- Support ring buffer area management
- Support peripherals: TIM/ADC/USART/I2C/SPI

- **12-bit ADC:**

- Conversion range: 0~V_{DDA}. The conversion is completed in1us at the fastest
- 16 external signal channels + 2 internal signal channels
- On-chip temperature sensor

- **16-channel touch-key channel detection**

- **7 timers:**

- 1×16-bit advanced-control timer, including general-purpose timer function, and provided with dead zone control and emergency brake, provide PWM for motor control
- 3×16-bit general-purpose timers, provide up to 4 channels for input capture/output comparison/PWM/pulse counting and incremental encoder input
- 2 watchdog timers (independent watchdog and

window watchdog)

- System time timer: 64-bit self-increment counter

- **8 standard communication interfaces:**

- USB2.0 host/device interface (full-speed and low-speed)
- 2 I2Cs (support SMBus/PMBus)
- 3 USARTs (support ISO7816 interface, LIN, IrDA interfaces and modem control)
- 2 SPIs (support Master and Slave modes)

- **Fast GPIO ports:**

- Up to 51 I/O ports
- Can map to 16 external interrupts

- **Security features:** CRC calculation unit, 96-bit unique ID
- **Debug mode:** 2-wire serial debug interface
- **Package**

- LQFP64M
- LQFP48
- QFN48×7

Chapter 1 Specification Information

CH32V103 series MCU products use QingKe microprocessor and support RV32IMAC open-source instructions. The highest operating frequency is 80MHz, with built-in high-speed memory, and prefetching is used to improve the instruction access speed. Multiple buses work synchronously in the system structure, which provides rich peripheral functions and enhanced I/O ports. This series of products have built-in functions such as RTC, clock security mechanism, a 12-bit ADC, multiple timers, 16-channel TKey, and standard communication interfaces: 2 I2C interfaces, 2 SPIs, 3 USARTs, and 1 USB2.0 full-speed host / device interface (full-/ low-speed communication). The power supply voltage of this series is 2.7V~5.5V, and the operating temperature range is-40 °C~85 °C industrial-grade. Support a variety of energy-saving operating modes to meet the requirements of low-power applications. The products in this series are different in resource allocation, number of peripherals, functions of peripherals and so on. Several packaging forms of LQFP64M/LQFP48/QFN48-7*7 are provided. Can be widely used in: motor drive and application control, medical and handheld devices, PC game peripherals and GPS platforms, programmable controllers, frequency converters, printers, scanners, alarm systems, video intercom, heating, ventilation and air conditioning systems and other occasions.

1.1 Comparison

Table 1-1 CH32V103x product resource allocation

Difference \ Product No.		CH32V103 C6T6	CH32V103 C8T6	CH32V103 C8U6	CH32V103 R8T6
Pin count		48	48	48	64
Flash memory (byte)		32K	64K	64K	64K
SRAM (byte)		10K	20K	20K	20K
Number of GPIOs		37	37	37	51
Timer	General-purpose	2	3	3	3
	Advanced	1	1	1	1
	Watchdog (WDT)	2	2	2	2
	SysTick	1	1	1	1
ADC/TKey (Number of channels)		10	10	10	16
Communication Interface	SPI	1	2	2	2
	I2C	1	2	2	2
	USART	2	3	3	3
	USBHD 2.0FS	1	1	1	1
CPU clock frequency		Typical: 72MHz			
Operating voltage		2.7V~5.5V			
Operating temperature		Industrial grade -40°C~85°C			
Package		LQFP48		QFN48×7	LQFP64M(10*10)

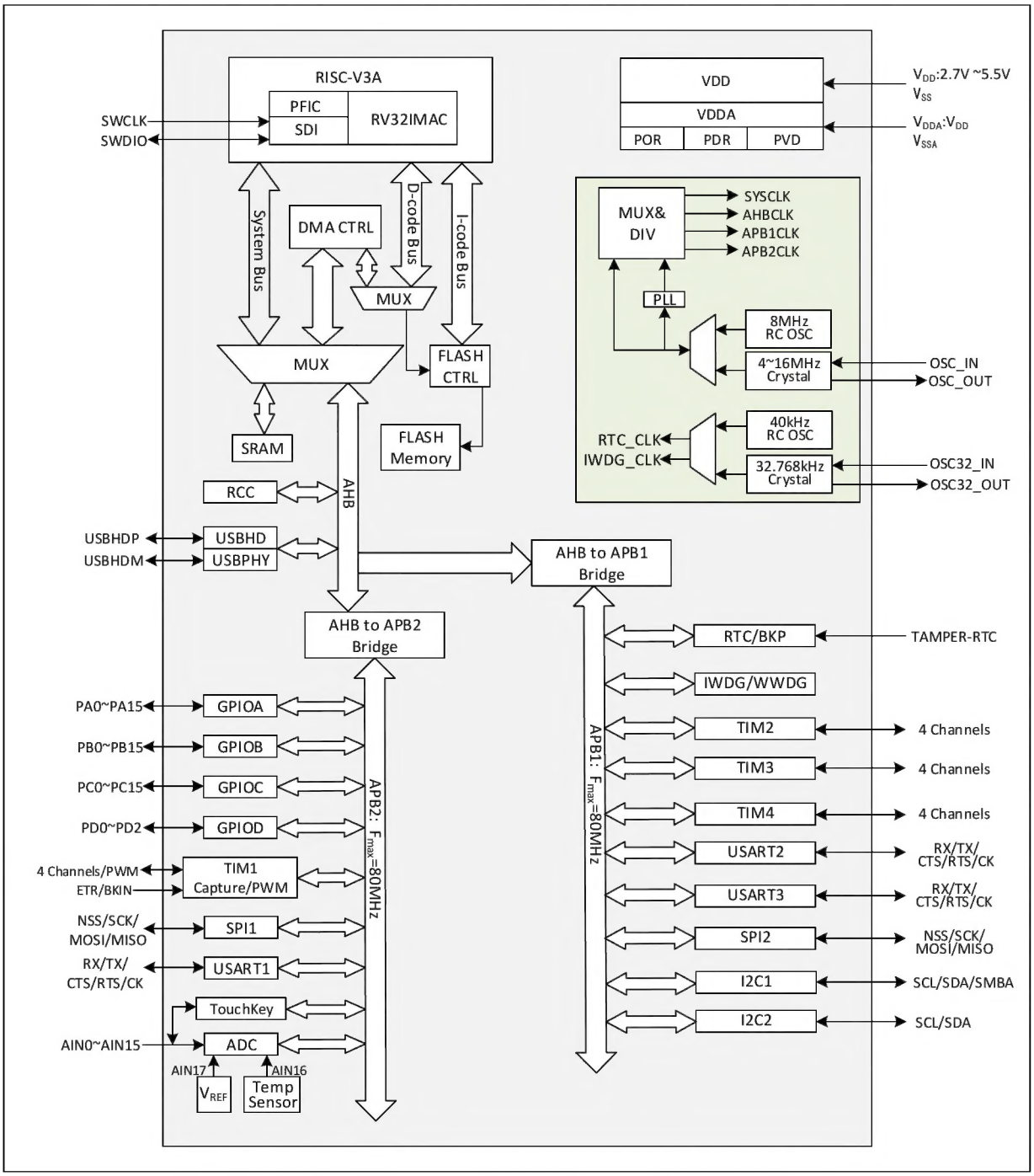
1.2 System Architecture

CH32V103 series products are general-purpose microcontrollers based on QingKe RISC-V3A processor. The core, arbitration unit, DMA module, SRAM storage and other parts of its architecture interact with each other through

multiple groups of buses. The core adopts pipeline processing structure and sets up static branch prediction and instruction prefetching mechanism to achieve the best performance ratio of low-power consumption, low-cost and high-speed operation of the system. There is a general DMA controller in the controller to reduce the burden of CPU and improve efficiency. Clock tree hierarchical management reduces the total power consumption of peripherals. At the same time, it also has data protection mechanism, clock security system protection mechanism and other measures to increase system stability.

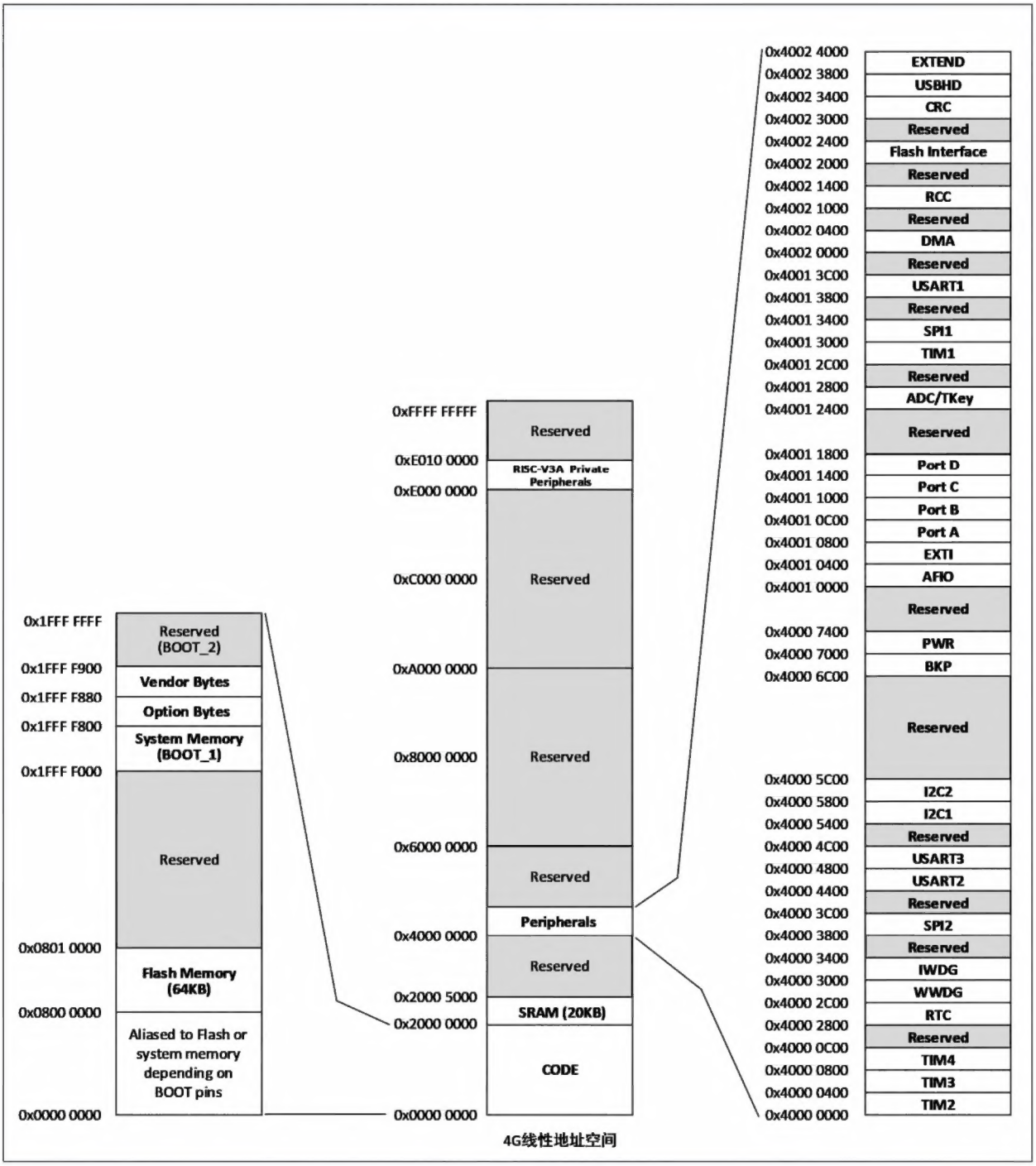
The following figure is the internal architecture block diagram of the series of products.

Figure 1-1 System architecture



1.3 Memory Mapping

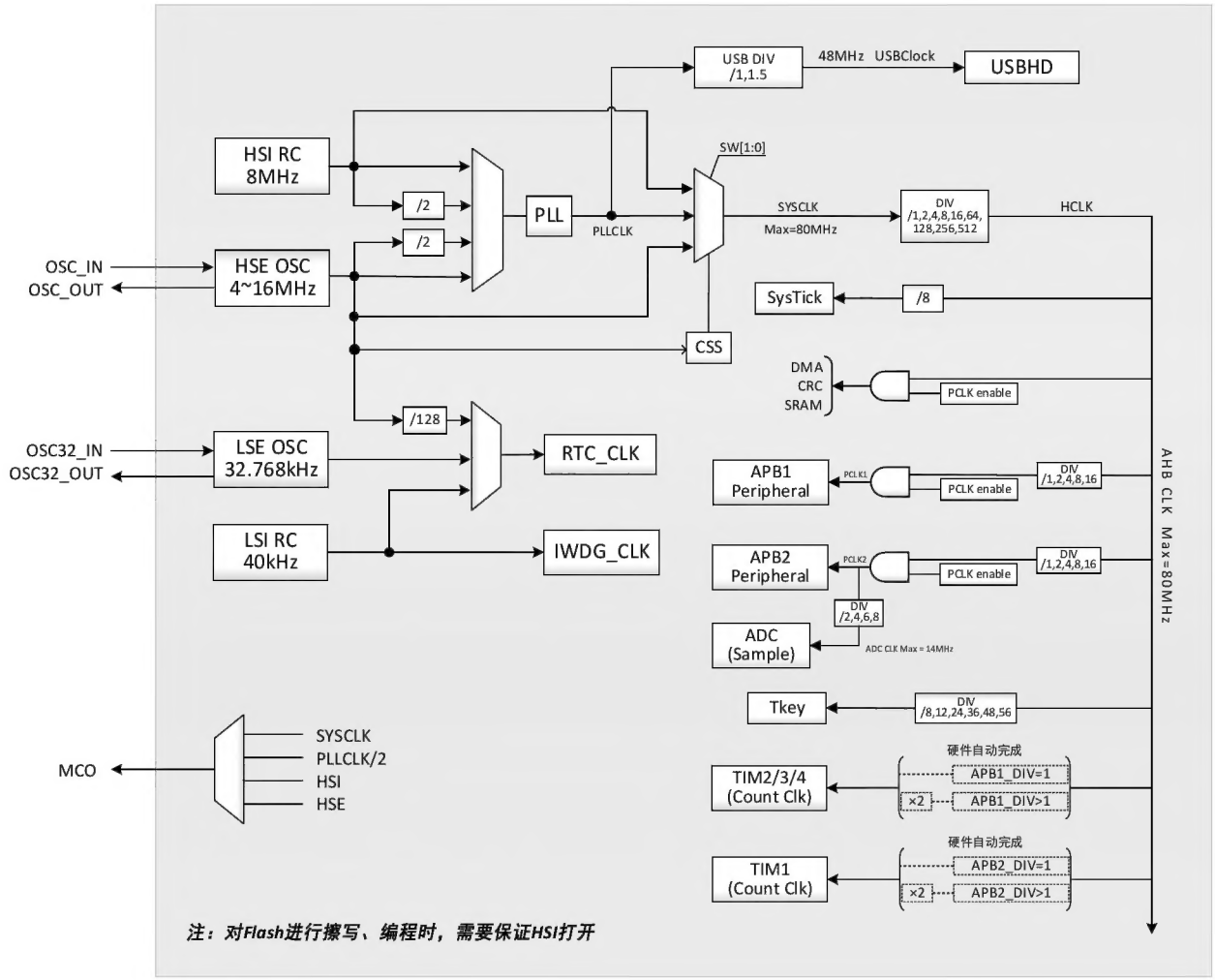
Figure 1-2 Memory address mapping



1.4 Clock Tree

The system provides four sets of clock sources: high-speed internal RC oscillator (HSI), low-speed internal RC oscillator (LSI), high-speed external oscillator or clock signal (HSE), low-speed external oscillator or clock signal (LSE). Wherein, the system bus clock (SYSCLK) comes from a high frequency clock source (HSI/HSE) or a higher clock generated after it is fed into the PLL frequency doubling. The AHB domain, APB1 domain and APB2 domain are obtained by the system clock or the previous stage through the corresponding prescaler frequency division.
The low frequency clock source provides a clock reference for RTC and independent watchdogs.
The PLL frequency doubling clock provides the working clock reference 48MHz of the USBHD module directly through the frequency divider.

Figure 1-3 Clock tree block diagram



Note:

1. When using USB function, the frequency of using PLL, CPU must be 48MHz or 72MHz at the same time.

2. When the ADC sampling time is 1us, APB2 must be set to 14MHz, 28MHz or 56MHz.

3. When the system wakes up from sleep, the system will automatically switch to HSI as the clock frequency.

4. When erasing, writing and programming Flash, you must make sure that HSI is open.

1.5 Functional Description

1.5.1 RISC-V3A Processor

RISC-V3A is a 32-bit embedded processor with internal modular management and supports the IMAC subset of the RISC-V open-source command set. It includes Programmable Fast Interrupt Controller (PFIC), provides 4 vector programmable fast interrupt channels and 44 priority configurable ordinary interrupts, and realizes the shortest cycle response of interrupts by means of hardware on-site storage and restoration. It includes 2-wire serial debug interface, supports user online upgrading and debugging. It includes multiple sets of buses connected to the external unit modules of processor to realize the interaction between external function modules and the core.

- RV32IMAC command set, small-end data mode
- Support machine and user privilege mode
- Programmable Fast Interrupt Controller (PFIC), Tail-Chaining interrupt processing, 2-level hardware stack
- 2-wire serial debug interface
- Branch prediction, efficient jump, conflict detection mechanism

The processor based on this design can be flexibly applied to microcontroller designs in different scenarios, such as small-area, low-power consumption embedded scenarios, and high-performance application operating system scenarios with its features such as minimal instruction set, multiple operating modes, and modular customization extension.

The CH32V1 series controller adopts the RISC-V3A core, is equipped with a complete software and hardware platform and tools, and supports online download, debugging, and tracking of application codes.

1.5.2 On-chip Memory and Boot Mode

Built-in 20 Kbytes of SRAM area is used to store the data.

Built-in 64 Kbytes of program flash memory storage area (CodeFlash) is used to store the user application program.

Built-in 3.75 Kbytes of system storage area (BootLoader) is used to store the system guidance programs (manufacturer's solidified boot loading program).

In addition, 128 bytes are used to store the manufacturer's configuration word and 128 bytes are used for saving the selection words by the user.

During the startup, one of three bootstrap modes can be selected through the boot pins (BOOT0 and BOOT1):

- Boot from the program flash memory
- Boot from the system memory
- Boot from the internal SRAM

The boot loading program is saved in the system storage area and the contents of the program flash memory storage area can be re-programmed through the USART1 and USB interfaces.

1.5.3 Power Supply Scheme

- V_{DD} = 2.7~5.5V: The V_{DD} pin supplies power to I/O pins, RC oscillator, reset module and internal voltage regulator.
- V_{DDA} = 2.7~5.5V: It supplies power to the simulation part of ADC, TS and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.
- V_{BAT} = 1.8~5.5V: When the V_{DD} is removed or does not work, V_{BAT} separately supplies power to RTC, external 32KHz oscillator and backup register.

1.5.4 Power Supply Supervisor

This product internally integrates a power-on reset (POR)/power-down reset (PDR) circuit, which is always in the working condition to ensure that the system works when the power supply exceeds 2.7V. When V_{DD} is lower than the set threshold ($V_{POR/PDR}$), place the device in the reset state, and an external reset circuit does not need to be used. In addition, there is a programmable voltage detector (PVD), which needs to be switched on by software to compare the voltage of V_{DD}/V_{DDA} power supply and the set threshold V_{PVD}. Open the corresponding edge interrupt of PVD. When the V_{DD} is reduced to PVD threshold or increased to PVD threshold, the interrupt notice will be received. Refer to Table 3-4 for the values of $V_{POR/PDR}$ and V_{PVD}.

1.5.5 Voltage Regulator

After reset, the regulator will be automatically switched on. There are three operating modes according to the application method.

- ON mode: The stable core power supply is provided through the normal operation
- Low power mode: After CPU enters Stop mode, you can select to operate the regulator at low-power consumption
- OFF mode: When CPU enters Standby mode, the regulator is automatically switched to OFF mode, the voltage regulator output is in high impedance, and the core circuitry is powered down, inducing zero consumption.

The voltage regulator is always ON after reset. It is OFF in Standby mode, and the voltage regulator output is in high impedance.

1.5.6 Low-power Mode

The series products support 3 low-power modes and can reach the optimum balance under the conditions of low power, short start time and multiple wake-up events.

- Sleep Mode

Enter Sleep mode by executing WFI/WFE command. In Sleep mode, only the CPU clock stops, but the power supply of all peripheral clocks is normal and the peripherals are working. This mode is the shallowest low-power mode, but can reach the fastest wake-up.

Exit conditions: Any interrupt or wake-up event.

- Stop mode

Clear the PDDS bit. Set the SLEEPDEEP bit. Reset/set the LPDS bit. Enter Stop mode by executing WFI/WFE command. In Stop mode, FLASH enters low-power mode, and LPDS bit decides whether the core part is powered down, and the RC oscillator of PLL and HSI and HSE crystal oscillator are switched off. In Stop mode, the power consumption can reach the lowest when the contents of SRAM and register are maintained not to be lost.

Exit conditions: Any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset and a rising edge on WKUP pin. EXTI signals include one of 16 external I/O ports, PVD output, RTC clock and USB wake-up signal.

- Standby mode

Set the PDDS and SLEEPDEEP bits. Enter Standby mode by executing WFI/WFE command. The core part is powered down. The RC oscillator and HSE crystal oscillator of PLL and HSI are also switched off. The minimum power consumption can be achieved in this mode, but the system will reset after wake-up.

Exit conditions: Any external interrupt/event (EXTI signal), external reset signal on NRST, IWDG reset and a rising edge on WKUP pin. EXTI signals include one of 16 external I/O ports, PVD output, RTC clock and USB wake-up signal.

1.5.7 Cyclic Redundancy Check (CRC) Calculation Unit

CRC (cyclic redundancy check) calculation unit uses a fixed polynomial generator to generate a CRC code from a 32-bit data word. In many applications, CRC based technology is used to verify the consistency of data transfer and storage. Within the scope of EN/ IEC 60335-1 standard, a method of detecting flash memory error is provided. The CRC calculation unit can be used to calculate software signature real-timely and it shall be compared with the signature generated when linking and generating the software.

1.5.8 Programmable Fast Interrupt Controller (PFIC)

The product has built-in fast programmable interrupt controller (FPIC), which supports up to 255 interrupt vectors. Ch32v1 controller provides 5 core private interrupts and 44 peripheral interrupt management, and other interrupt sources are reserved. FPIC registers can be accessed in both user and machine privilege modes.

- 44 + 3 separate maskable interrupts
- Providing a non-maskable interrupt NMI
- 16-level priority programming, modified dynamically.
- For 2-level nesting interrupt entry and exit and hardware automatic stacking and recovery; no instruction overhead is required
- 4-channel programmable fast interrupt channel; custom interrupt vector address
- Support interrupt tail link function
- Provide the prompt response of non-maskable interrupt

The module provides flexible interrupt management with minimal interrupt delay.

1.5.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains 20 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently to select the corresponding trigger event (rising or falling or both), and can be masked independently. The pending register maintains all interrupt request states. EXTI can detect the external signal with pulse width lower than internal APB2 clock period. Up to 51 general-purpose I/O ports can be selectively connected to 16 external interrupt lines.

1.5.10 General-purpose DMA Controller

Flexible general-purpose DMA can manage the high-speed data transfer from memory to memory, peripheral to memory and memory to peripheral, providing 7 channels and supporting ring buffer area management. Each channel has special hardware DMA request logic, which supports the access request of one or more peripheral devices to the memory and data transfer from memory to memory. The access priority, transfer length, source address and destination address of transmission can be configured.

The main peripherals used in DMA include: General-purpose/advanced-control timers TIM, ADC, USART, I2C, and SPI.

1.5.11 Clock and Startup

The system clock source HSI is on by default. After no clock is configured or reset, the internal 8MHz RC oscillator will be used as the default CPU clock, and then the external 4-16MHz clock or PLL clock can be selected. After the clock safety mode is switched on, if HSE is used as the system clock (directly or indirectly), the system clock will be automatically switched to the internal RC oscillator and HSE and PLL will be automatically turned off when the system detects the external clock failure; for the low power consumption mode of switching off the clock, the system will also automatically switch to the internal RC oscillator after wake-up. If the clock interrupt is enabled, the

software can receive corresponding interrupt.
Several prescalers are used to configure AHB bus clock, high-speed APB2 and low-speed APB1 area bus clock. Refer to Figure 1-2 Clock tree block diagram.

1.5.12 Real-time Clock (RTC) and Backup Register

The RTC and backup register are in the backup power supply domain inside the product. When the V_{DD} is valid, the power will be supplied by the V_{DD}. Otherwise, the V_{BAT} pin will be automatically switched internally to supply the power.
RTC real-time clock is a group of 32-bit programmable counters. The time base supports 20-bit prescaler, which is used for the measurement in the long period. The clock reference source is high-speed external clock divided by 128 (HSE/128), 32.768 KHz oscillator (LSE) of external crystal or internal low-power RC oscillator (LSI). The LSE also has a backup power supply domain. Therefore, when LSE is selected as RTC time base, the setting and time of RTC can remain unchanged after the system is reset or woken up from the standby mode.
The backup register includes ten 16-bit registers, which can be used to store 20 bytes of user application data. The data can be maintained and will not be reset after the standby wake-up, or when the system is reset or the power is reset. When the intrusion detection function is switched on, once the intrusion detection signal is valid, all contents in the backup register can be cleared.

1.5.13 Analog-to-digital Converter (ADC) and Capacitive Touch-key Detection (Tkey)

The product has a built-in 12-bit ADC that provides up to 16 external channels and 2 internal channel samples with programmable channel sampling time for single, continuous, scan or discontinuous mode conversion. The analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages. External event trigger conversion is supported, and the trigger source includes the internal signal of the on-chip timer and the external pin (EXTI line 11). Support the use of DMA operations.
The ADC internal channel sampling includes 1-channel built-in temperature sensor sampling and 1-channel internal reference power sampling. The temperature sensor generates a voltage that varies linearly with temperature, and the power supply range is 3.0V $<V_{DDA}<$ 5.5V. The temperature sensor is internally connected to the ADC_ IN16 input channel, used to convert the output of the sensor to a digital value.
The capacitive touch-key detection function multiplexes the external channel of ADC to provide up to 16 circuits of detection. The application program judges the status of touch-key based on the change of digital value.

1.5.14 Timer

The timer consists of an advanced 16-bit timer, 3 general-purpose 16-bit timers, 2 watchdog timers and a system time base timer.

1.5.14.1 Advanced-control Timer (TIM1)

The advanced-control timer (TIM1) is a 16-bit automatic loading counter with a programmable prescaler. In addition to the complete general timer function, it can be regarded as a three-phase PWM generator assigned to six channels, having the complementary PWM output function with dead zone insertion. The timer allows to be updated after a specified number of counter cycles for repeated counting cycle and braking function, etc. Many functions of advanced control timer are the same as those of general timer, and the internal structure is also the same. Therefore, advanced control timer can operate with TIM timer through timer link function to provide synchronization or event linking function.

1.5.14.2 General-purpose timer (TIM2/3/4)

The system provides up to 3 standard timers (TIM2, TIM3 and TIM4) which can be operated synchronously. Each timer has a 16-bit auto-load increment/decrement counter, a programmable 16-bit prescaler and 4 independent channels, each of which can be used for input capture, output comparison, PWM generation and single pulse mode output.

It can also work with advanced-control timer through timer link function to provide synchronization or event linking function. In the debug mode, the counter can be frozen and the PWM output is disabled, thus switching off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has its own DMA request mechanism.

These timers can also process signals from incremental encoders and digital outputs from 1 to 3 Hall sensors.

1.5.14.3 Independent Watchdog (IWDG)

The independent watchdog is a free running 12-bit down counter with an 8-bit prescaler. The clock is provided by an internally independent 40KHz RC oscillator; since this RC oscillator is independent of the master clock, it can operate in stop and standby modes. IWDG completely works independently of the main program, so it can be used to reset the whole system in case of problems, or to provide timeout management for applications as a free timer. The option byte can be configured as a software or hardware boot watchdog. In the debug mode, the counter can be frozen.

1.5.14.4 Window Watchdog (WWDG)

The window watchdog is a 7-bit down counter and can be set to run freely. It can be used to reset the entire system in the event of a problem. It is driven by the master clock and has the function of early warning interrupt. In the debug mode, the counter can be frozen.

1.5.14.5 System Time Base Timer (SysTick)

This is a timer provided by the core controller to generate SYSTICK exception. It can be used in real-time operating system to provide "heartbeat" rhythm for the system. It can also be used as a standard 64-bit increment counter. The 8 frequency divisions of AHB clock are used as the reference clock sources. When the counter is increased to the set comparison value, a maskable system interrupt is generated.

1.5.15 Universal Synchronous Asynchronous Receiver Transmitter (USART)

3 groups of USARTs support full-duplex asynchronous communication, synchronous one-way communication, half duplex single line communication and Lin (local Internet), and are compatible with ISO7816 smart card protocol, IrDA SIR ENDEC transfer encoder/decoder specifications, and modem (CTS/RTS hardware flow control) operation. The multi-processor communication is also supported. The fractional baud rate generator system is used. The baud rate of USART1 can be up to 4.5 Mbits/s, and baud rate of USART2/3 can be up to 2.25 Mbits/s. They support DMA operation for continuous communication.

1.5.16 Serial Peripheral Interface (SPI)

2 sets of SPIs provide the master/slave operation and are switched dynamically. They support multi-master mode, full duplex or half duplex synchronous transfer, and support basic SD card and MMC mode. The clock frequency can be up to 36 MHz, clock polarity and phase are programmable, 8-bit or 16-bit data bit width can be selected, the hardware CRC generation/verification is reliable. They support DMA operation for continuous communication.

1.5.17 I2C Bus

Up to 2 I2C interfaces can work in multi-master mode and slave mode and can complete specific timing, protocol, arbitration, etc. for all I2C buses. They support standard communication speed and fast communication speed, and are compatible with SMBus2.0.

I2Cs provide 7-bit or 10-bit addressing, and support dual-slave addressing in 7-bit slave mode. The built-in hardware CRC generator/calibrator is provided. DMA operation can be used, SMBus2.0/PMBus are supported.

1.5.18 Universal Serial Bus (USB)

The product has built-in a USB2.0 host controller and device controller (USBHD), which comply with USB2.0 Fullspeed Standard. It provides 16 configurable USB device endpoints and a set of host endpoint. It supports control/bulk/isochronous/interrupt transfer, double-buffered mechanism, USB Suspend/Resume operations, and provides standby/wake-up function. The dedicated 48 MHz clock of USBHD module is directly generated by internal main PLL divider (PLL must be 72 MHz or 48 MHz).

1.5.19 General-purpose Input/Output (GPIO)

The system provides 4 groups of GPIO ports with 51 GPIO pins in total. Each pin can be configured as an output (push-pull or open drain), an input (with or without pull-up or pull-down) or a multiplexed peripheral function port by software. Most GPIO pins can be shared with digital or analog multiplexed peripherals. Except for the ports with analog input function, all GPIO pins have high current carrying capacity. It provides a locking mechanism to freeze IO configuration to avoid accidental writing to I/O register.

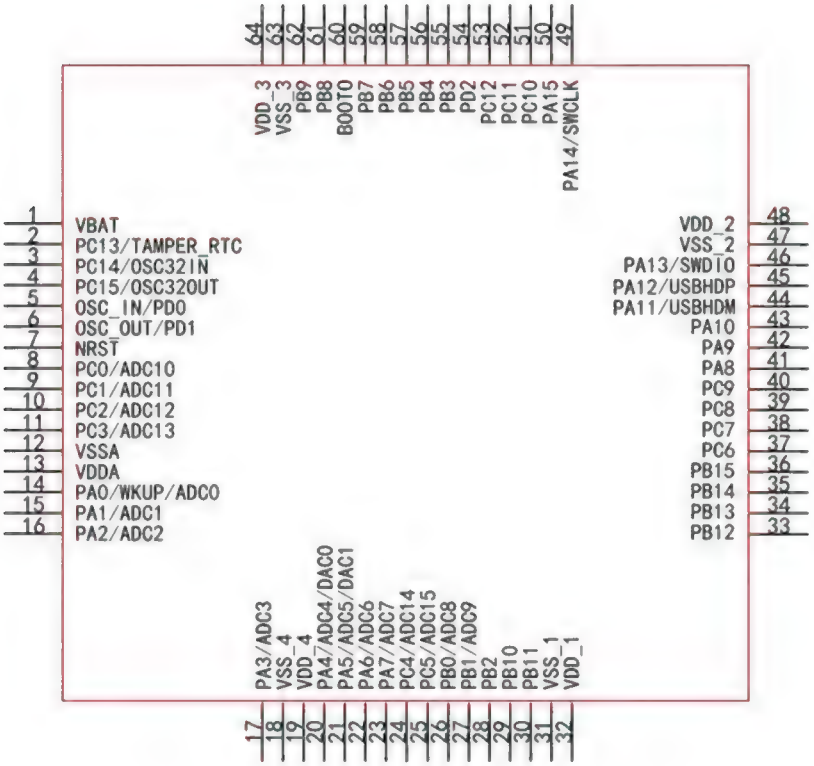
1.5.20 2-wire Serial Debug Interface (SDI)

The core comes with a serial 2-wire debugging interface (SDI), including SWDIO and SWCLK pins. By default, the debugging interface pins are turned on after the system is powered on or reset, and the SDI can be turned off as needed after the main program is run.

Chapter 2 Pinouts and Pin Definitions

2.1 Pinouts

CH32V103R8T6



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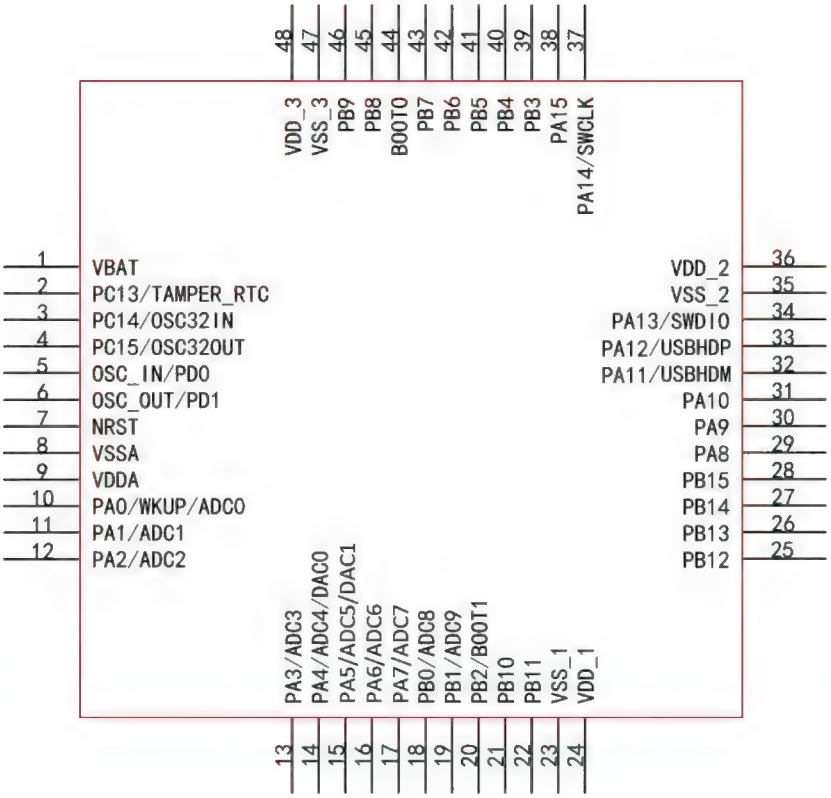


2.2 Pin Definitions

Note that the pin function description in the following table is for all functions and does not involve specific model products. There are differences in peripheral resources between different models. Please confirm this function according to the product model resource table before checking.

Table 2-1 CH32V103x8x6 pin definitions

Pin No.			Pin Name	Pin Type (1)	Main function (after reset)	Default alternate function	Remapping function (2)
LQFP48	QFN48×7	LQFP64M					
1	1	1	V_{BAT}	P	V_{BAT}		
2	2	2	PC13-TAMPER-RTC(3)	I/O	PC13	TAMPER-RTC	
3	3	3	PC14-OSC32_IN(3)	I/O/A	PC14	OSC32_IN	
4	4	4	PC15-OSC32_OUT(3)	I/O/A	PC15	OSC32_OUT	
5	5	5	OSC_IN	I/A	OSC_IN		PD0(4)
6	6	6	OSC_OUT	O/A	OSC_OUT		PD1(4)
7	7	7	NRST	I/O	NRST		
-	-	8	PC0	I/O/A	PC0	ADC_IN10	
-	-	9	PC1	I/O/A	PC1	ADC_IN11	
-	-	10	PC2	I/O/A	PC2	ADC_IN12	
-	-	11	PC3	I/O/A	PC3	ADC_IN13	
8	8	12	V_{SSA}	P	V_{SSA}		
9	9	13	V_{DDA}	P	V_{DDA}		
10	10	14	PA0-WKUP	I/O/A	PA0	WKUP/USART2_CTS/ADC_IN0/ TIM2_CH1/TIM2_ETR	
11	11	15	PA1	I/O/A	PA1	USART2_RTS/ADC_IN1/ TIM2_CH2	
12	12	16	PA2	I/O/A	PA2	USART2_TX/ADC_IN2/ TIM2_CH3	
13	13	17	PA3	I/O/A	PA3	USART2_RX/ADC_IN3/ TIM2_CH4	
-	-	18	V_{SS_4}	P	V_{SS_4}		
-	-	19	V_{DD_4}	P	V_{DD_4}		
14	14	20	PA4	I/O/A	PA4	SPI1_NSS/USART2_CK/ ADC_IN4	
15	15	21	PA5	I/O/A	PA5	SPI1_SCK/ADC_IN5	
16	16	22	PA6	I/O/A	PA6	SPI1_MISO/ADC_IN6/ TIM3_CH1	TIM1_BKIN_1

17	17	23	PA7	I/O/A	PA7	SPI1_MOSI/ADC_IN7/ TIM3_CH2	TIM1_CH1N_1
-	-	24	PC4	I/O/A	PC4	ADC_IN14	
-	-	25	PC5	I/O/A	PC5	ADC_IN15	
18	18	26	PB0	I/O/A	PB0	ADC_IN8/TIM3_CH3	TIM1_CH2N_1
19	19	27	PB1	I/O/A	PB1	ADC_IN9/TIM3_CH4	TIM1_CH3N_1
20	20	28	PB2	I/O	PB2 /BOOT1		
21	21	29	PB10	I/O	PB10	I2C2_SCL/USART3_TX	TIM2_CH3_1
22	22	30	PB11	I/O	PB11	I2C2_SDA/USART3_RX	TIM2_CH4_1
23	23	31	V_{SS_1}	P	V_{SS_1}		
24	24	32	V_{DD_1}	P	V_{DD_1}		
25	25	33	PB12	I/O	PB12	SPI2_NSS/I2C2_SMBAI/ USART3_CK/TIM1_BKIN	
26	26	34	PB13	I/O	PB13	SPI2_SCK/USART3_CTS/ TIM1_CH1N	
27	27	35	PB14	I/O	PB14	SPI2_MISO/USART3_RTS/ TIM1_CH2N	
28	28	36	PB15	I/O	PB15	SPI2_MOSI/TIM1_CH3N	
-	-	37	PC6	I/O	PC6		TIM3_CH1_1
-	-	38	PC7	I/O	PC7		TIM3_CH2_1
-	-	39	PC8	I/O	PC8		TIM3_CH3_1
-	-	40	PC9	I/O	PC9		TIM3_CH4_1
29	29	41	PA8	I/O	PA8	USART1_CK/TIM1_CH1/MCO	
30	30	42	PA9	I/O	PA9	USART1_TX/TIM1_CH2	
31	31	43	PA10	I/O	PA10	USART1_RX/TIM1_CH3	
32	32	44	PA11	I/O/A	PA11	USART1_CTS/USBHDM/TIM1_CH4	
33	33	45	PA12	I/O/A	PA12	USART1_RTS/USBHDP/TIM1_ETR	
34	34	46	PA13	I/O	SWDIO		PA13(5)
35	35	47	V_{SS_2}	P	V_{SS_2}		
36	36	48	V_{DD_2}	P	V_{DD_2}		
37	37	49	PA14	I/O	SWCLK		PA14(5)
38	38	50	PA15	I/O	PA15		TIM2_CH1_1/ TIM2_ETR_1/ SPI1_NSS_1
-	-	51	PC10	I/O	PC10		USART3_TX_1
-	-	52	PC11	I/O	PC11		USART3_RX_1
-	-	53	PC12	I/O	PC12		USART3_CK_1
-	-	54	PD2	I/O	PD2	TIM3_ETR	
39	39	55	PB3	I/O	PB3		TIM2_CH2_1/ SPI1_SCK_1
40	40	56	PB4	I/O	PB4		TIM3_CH1_1/ SPI1_MISO_1

41	41	57	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2_1/ SPI1_MOSI_1
42	42	58	PB6	I/O/A	PB6	I2C1_SCL/TIM4_CH1	USART1_TX_1
43	43	59	PB7	I/O/A	PB7	I2C1_SDA/TIM4_CH2	USART1_RX_1
44	44	60	BOOT0	I	BOOT0		
45	45	61	PB8	I/O/A	PB8	TIM4_CH3	I2C1_SCL_1
46	46	62	PB9	I/O/A	PB9	TIM4_CH4	I2C1_SDA_1
47	47	63	V_{SS_3}	P	V_{SS_3}		
48	48	64	V_{DD_3}	P	V_{DD_3}		

Table 2-2 CH32V103x6x6 pin definitions

Pin No.		Pin Name	Pin Type (1)	Main function (after reset)	Default alternate function	Remapping function (2)
LQFP48	LQFP64M					
1	1	V_{BAT}	P	V_{BAT}		
2	2	PC13-TAMPER-RTC(3)	I/O	PC13	TAMPER-RTC	
3	3	PC14-OSC32_IN(3)	I/O/A	PC14	OSC32_IN	
4	4	PC15-OSC32_OUT(3)	I/O/A	PC15	OSC32_OUT	
5	5	OSC8M_IN	I/A	OSC8M_IN		PD0(4)
6	6	OSC8M_OUT	O/A	OSC8M_OUT		PD1(4)
7	7	NRST	I/O	NRST		
-	8	PC0	I/O/A	PC0	ADC_IN10	
-	9	PC1	I/O/A	PC1	ADC_IN11	
-	10	PC2	I/O/A	PC2	ADC_IN12	
-	11	PC3	I/O/A	PC3	ADC_IN13	
8	12	V_{SSA}	P	V_{SSA}		
9	13	V_{DDA}	P	V_{DDA}		
10	14	PA0-WKUP	I/O/A	PA0	WKUP/USART2_CTS/ADC_IN0/ TIM2_CH1/TIM2_ETR	
11	15	PA1	I/O/A	PA1	USART2_RTS/ADC_IN1/ TIM2_CH2	
12	16	PA2	I/O/A	PA2	USART2_TX/ADC_IN2/TIM2_CH3	
13	17	PA3	I/O/A	PA3	USART2_RX/ADC_IN3/TIM2_CH4	
-	18	V_{SS_4}	P	V_{SS_4}		
-	19	V_{DD_4}	P	V_{DD_4}		
14	20	PA4	I/O/A	PA4	SPI1_NSS/USART2_CK/ADC_IN4	
15	21	PA5	I/O/A	PA5	SPI1_SCK/ADC_IN5	
16	22	PA6	I/O/A	PA6	SPI1_MISO/ADC_IN6/TIM3_CH1	TIM1_BKIN_1

17	23	PA7	I/O/A	PA7	SPI1_MOSI/ADC_IN7/TIM3_CH2	TIM1_CH1N_1
-	24	PC4	I/O/A	PC4	ADC_IN14	
-	25	PC5	I/O/A	PC5	ADC_IN15	
18	26	PB0	I/O/A	PB0	ADC_IN8/TIM3_CH3	TIM1_CH2N_1
19	27	PB1	I/O/A	PB1	ADC_IN9/TIM3_CH4	TIM1_CH3N_1
20	28	PB2	I/O	PB2/BOOT1		
21	29	PB10	I/O	PB10		TIM2_CH3_1
22	30	PB11	I/O	PB11		TIM2_CH4_1
23	31	V_{SS_1}	P	V_{SS_1}		
24	32	V_{DD_1}	P	V_{DD_1}		
25	33	PB12	I/O	PB12	TIM1_BKIN	
26	34	PB13	I/O	PB13	TIM1_CH1N	
27	35	PB14	I/O	PB14	TIM1_CH2N	
28	36	PB15	I/O	PB15	TIM1_CH3N	
-	37	PC6	I/O	PC6		TIM3_CH1_1
-	38	PC7	I/O	PC7		TIM3_CH2_1
-	39	PC8	I/O	PC8		TIM3_CH3_1
-	40	PC9	I/O	PC9		TIM3_CH4_1
29	41	PA8	I/O	PA8	USART1_CK/TIM1_CH1/MCO	
30	42	PA9	I/O	PA9	USART1_TX/TIM1_CH2	
31	43	PA10	I/O	PA10	USART1_RX/TIM1_CH3	
32	44	PA11	I/O/A	PA11	USART1_CTS/USBHDM/TIM1_CH4	
33	45	PA12	I/O/A	PA12	USART1_RTS/USBHDP/TIM1_ETR	
34	46	PA13	I/O	SWDIO		PA13(5)
35	47	V_{SS_2}	P	V_{SS_2}		
36	48	V_{DD_2}	P	V_{DD_2}		
37	49	PA14	I/O	SWCLK		PA14(5)
38	50	PA15	I/O	PA15		TIM2_CH1_1/ TIM2_ETR_1/ SPI1_NSS_1
-	51	PC10	I/O	PC10		
-	52	PC11	I/O	PC11		
-	53	PC12	I/O	PC12		
-	54	PD2	I/O	PD2	TIM3_ETR	
39	55	PB3	I/O	PB3		TIM2_CH2_1/ SPI1_SCK_1
40	56	PB4	I/O	PB4		TIM3_CH1_1/ SPI1_MISO_1

41	57	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2_1/ SPI1_MOSI_1
42	58	PB6	I/O/A	PB6	I2C1_SCL	USART1_TX_ 1
43	59	PB7	I/O/A	PB7	I2C1_SDA	USART1_RX_ 1
44	60	BOOT0	I	BOOT0		
45	61	PB8	I/O/A	PB8		I2C1_SCL_1
46	62	PB9	I/O/A	PB9		I2C1_SDA_1
47	63	V_{SS_3}	P	V_{SS_3}		
48	64	V_{DD_3}	P	V_{DD_3}		

Note 1: Pin Type:

I=TTL/CMOS Schmitt input; O=CMOS three-state output;

A=Analog signal input or output; P= Power.

Note 2: The value after the underscore of the remap function indicates the configuration value of the corresponding bit in the AFIO register. For example: TIM1_BKIN_1 indicates that the corresponding bit in the AFIO register is configured as 01b.

Note 3: When the backup domain is powered by V_{DD} (internal analog switch connected to V_{DD}): PC14 and PC15 can be used for GPIO or LSE pins, PC13 can be used as a GPIO, a TAMPER pin, an RTC calibration clock, an RTC alarm clock, or a second output; when used as an output pin, it can only work in the 2MHz mode with a maximum drive load of 30pF; when the backup domain is powered by V_{BAT} (analog switch connected to BAT after V_{DD} disappears): PC14 and PC15 can only be used for LSE pin, PC13 can be used as TAMPER pin, RTC alarm clock or seconds output.

Note 4: For CH32V103 chip, pin 5 and pin 6 are configured as OSC_IN and OSC_OUT function pins by default after chip reset. Software can reset these two pins to PD0 and PD1 functions. For more detailed information, please refer to the Multiplexed Function I/O section and the Debug Setup section of the CH32xRM manual.

Note 5: For the CH32V103R8T6 chip, pin 46 and pin 49 are configured as SWDIO and SWCLK function pins by default after chip reset. Software can reset these two pins for PA13 and PA14 functions; for CH32V103C6T6, CH32V103C8T6 and CH32V103C8U6 chips, pin 34 and pin 37 are configured as SWDIO and SWCLK function pins by default after chip reset. Software can reset these two pins to function as PA13 and PA14. Refer to the Multiplexed Function I/O section and the Debug Setup section of the CH32xRM manual for more details.

2.3 Pin Alternate Functions

Note: The pin function in the table below refer to all functions and does not involve specific model(s). There are differences in peripheral resources between different models. Please confirm whether this function is available according to the particular model's resource table before viewing this table.

Table 2-2 Pin alternate and remapping functions

Pin \ Alternate	ADC	TIM1	TIM2/3/4	USART	SYS	I2C	SPI	USB
PA0	ADC_IN0		TIM2_CH1 TIM2_ETR	USART2_CTS	WKUP			
PA1	ADC_IN1		TIM2_CH2	USART2_RTS				
PA2	ADC_IN2		TIM2_CH3	USART2_TX				
PA3	ADC_IN3		TIM2_CH4	USART2_RX				
PA4	ADC_IN4			USART2_CK			SPI1_NSS	
PA5	ADC_IN5						SPI1_SCK	
PA6	ADC_IN6	TIM1_BKIN_1	TIM3_CH1				SPI1_MISO	
PA7	ADC_IN7	TIM1_CH1N_1	TIM3_CH2				SPI1_MOSI	
PA8		TIM1_CH1		USART1_CK	MCO			
PA9		TIM1_CH2		USART1_TX				
PA10		TIM1_CH3		USART1_RX				
PA11		TIM1_CH4		USART1_CTS				USBHDM
PA12		TIM1_ETR		USART1_RTS				USBHDP
PA13					SWDIO			
PA14					SWCLK			
PA15			TIM2_CH1_1 TIM2_ETR_1				SPI1_NSS_1	
PB0	ADC_IN8	TIM1_CH2N_1	TIM3_CH3					
PB1	ADC_IN9	TIM1_CH3N_1	TIM3_CH4					
PB2					BOOT1			
PB3			TIM2_CH2_1				SPI1_SCK_1	
PB4			TIM3_CH1_1				SPI1_MISO_1	
PB5			TIM3_CH2_1			I2C1_SMBAI	SPI1_MOSI_1	
PB6			TIM4_CH1	USART1_TX_1		I2C1_SCL		
PB7			TIM4_CH2	USART1_RX_1		I2C1_SDA		
PB8			TIM4_CH3			I2C1_SCL_1		
PB9			TIM4_CH4			I2C1_SDA_1		
PB10			TIM2_CH3_1	USART3_TX		I2C2_SCL		
PB11			TIM2_CH4_1	USART3_RX		I2C2_SDA		
PB12		TIM1_BKIN		USART3_CK		I2C2_SMBAI	SPI2_NSS	
PB13		TIM1_CH1N		USART3_CTS			SPI2_SCK	
PB14		TIM1_CH2N		USART3_RTS			SPI2_MISO	
PB15		TIM1_CH3N					SPI2_MOSI	
PC0	ADC_IN10							
PC1	ADC_IN11							
PC2	ADC_IN12							
PC3	ADC_IN13							
PC4	ADC_IN14							
PC5	ADC_IN15							
PC6			TIM3_CH1_1					
PC7			TIM3_CH2_1					
PC8			TIM3_CH3_1					

Pin \ Alternate	ADC	TIM1	TIM2/3/4	USART	SYS	I2C	SPI	USB
PC9			TIM3_CH4_1					
PC10				USART3_TX_1				
PC11				USART3_RX_1				
PC12				USART3_CK_1				
PC13					TAMPER-RTC			
PC14					OSC32_IN			
PC15					OSC32_OUT			
PD0					OSC_IN			
PD1					OSC_OUT			
PD2			TIM3_ETR					

Chapter 3 Electrical Characteristics

3.1 Test Conditions

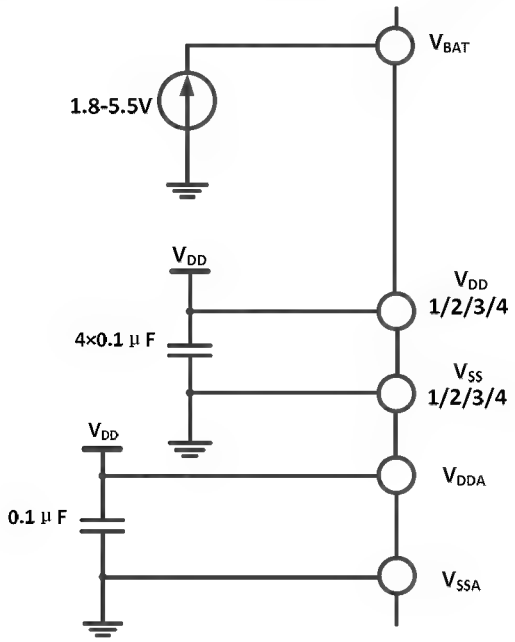
Unless otherwise specified and indicated, all voltages are referenced to V_{SS}.

All minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency. Typical values are based on normal temperature (25°C) and V_{DD} = 3.3V environment, which are given only as design guidelines.

The data based on comprehensive evaluation, design simulation or technology characteristics are not tested in production. On the basis of comprehensive evaluation, the minimum and maximum values refer to sample tests. Unless otherwise specified that is tested, the characteristic parameters are guaranteed by comprehensive evaluation or design.

Power supply scheme:

Figure 3-1 Typical circuit for conventional power supply



3.2 Absolute Maximum Ratings

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Table 3-1 Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
T_A(1)	Operating ambient temperature	-40	85	°C
T_S	Storage ambient temperature	-40	105	°C
V_{DD}-V_{SS}(1)	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	5.5	V
V_{IN}(1)	Input voltage on pins	V_{SS}-0.3	5.5	V
$\lvert\triangle V_{DDx}\rvert$(1)	Variations between different power pins		50	mV
$\lvert V_{SSx}-V_{SS}\rvert$(1)	Variations between different ground pins		50	mV
$V_{ESD(HBM)}$ (1)	ESD voltage (human body model, non-contact type)	4000		V
I_{VDD}(2)	Total current into V_{DD}/V_{DDA} power lines (source)		50	mA

I_{Vss}(2)	Total current out of V_{SS} ground lines (sink)		50	
I_{IO}(1)	Input current on any I/O and control pin		-25	
	Output current on any I/O and control pin		25	

Notes: 1. Parameters are guaranteed by design.

2. The maximum current value can be reached in normal operation.

3.3 Electrical Characteristics

3.3.1 Operating Conditions

Table 3-2 General operating conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
F_{SYSCLK}	Internal system clock frequency			80	MHz
F_{HCLK}	Internal AHB clock frequency			80	MHz
F_{PCLK1}	Internal APB1 clock frequency			80	MHz
F_{PCLK2}	Internal APB2 clock frequency			80	MHz
V_{DD}	Standard operating voltage		2.7	5.5	V
V_{DDA}	Analog operating voltage (ADC is not used)	Must be the same potential as V_{DD}.	2.7	5.5	V
	Analog operating voltage (ADC is used)		3.0		
V_{BAT} (2)	Backup operating voltage	Cannot be more than V_{DD}	1.8	5.5	V
T_A (1)	Ambient temperature		-40	85	℃

Notes: 1. Parameters are guaranteed by design.

2. The connecting line from the battery to V_{BAT} shall be as short as possible.

Table 3-3 Power-on and power-down conditions

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDD}	V_{DD} rise time rate		0	∞	us/V
	V_{DD} fall time rate		30	∞	

Note: The connecting line from the battery to N_{BAT} shall be as short as possible.

3.3.2 Built-in Reset and Power Control Module Characteristics

Table 3-4 Reset and voltage monitor (For PDR, select high threshold gear)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{PVD}(2)	Level selection of programmable voltage detector	PLS[2:0] = 000(rising edge)		2.65		V
		PLS[2:0] = 000(falling edge)		2.5		V
		PLS[2:0] = 001(rising edge)		2.87		V
		PLS[2:0] = 001(falling edge)		2.7		V
		PLS[2:0] = 010(rising edge)		3.07		V
		PLS[2:0] = 010(falling edge)		2.89		V
		PLS[2:0] = 011(rising edge)		3.27		V
		PLS[2:0] = 011(falling edge)		3.08		V

		PLS[2:0] = 100(rising edge)		3.46		V
		PLS[2:0] = 100(falling edge)		3.27		V
		PLS[2:0] = 101(rising edge)		3.76		V
		PLS[2:0] = 101(falling edge)		3.55		V
		PLS[2:0] = 110(rising edge)		4.07		V
		PLS[2:0] = 110(falling edge)		3.84		V
		PLS[2:0] = 111(rising edge)		4.43		V
		PLS[2:0] = 111(falling edge)		4.18		V
$V_{PVDhyst}$(1)	PVD hysteresis			0.2		V
$V_{POR/PDR}$(1)	Power-on/power-down reset threshold	Rising edge		2.5		V
		Falling edge		2.42		V
$V_{PDRhyst}$(1)	PDR hysteresis		40		110	mV
$t_{RSTTEMPO}$(1)	Reset duration		16		44	mS

Note: 1. Design parameters;

2. Normal temperature test value.

3.3.3 Built-in Reference Voltage

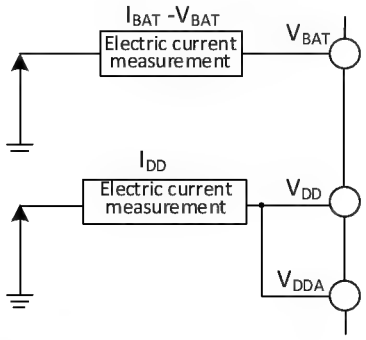
Table 3-5 Built-in reference voltage

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{REFINT}	Built-in reference voltage	T_A = -40°C ~ 85°C	1.12	1.28	V
$T_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	Slow sampling recommended	0.107	17.1	$1/f_{ADC}$

3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2 Current consumption measurement



The microcontroller is in the following conditions:

In the case of normal temperature VDD=3.3V, during the test: all IO ports are configured with pull-up input, enabling or turning off all peripheral clocks (excluding GPIO peripherals), and no peripheral function is initialized.

Table 3-6 Typical current consumption in Run mode, code with data processing running from internal flash memory

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(1)(2)	Supply current in Run mode	External clock	F_{SYSCLK} = 72MHz	13.56	8.88	mA
			F_{SYSCLK} = 48MHz	9.76	6.64	
			F_{SYSCLK} = 36MHz	8.51	5.85	
			F_{SYSCLK} = 24MHz	6.38	4.62	
			F_{SYSCLK} = 16MHz	5.11	3.88	
			F_{SYSCLK} = 8MHz	3.15	2.61	
			F_{SYSCLK} = 4MHz	2.50	2.26	
			F_{SYSCLK} = 500KHz	1.99	1.96	
		Runs in a high-speed internal RC oscillator (HSI), using AHB pre-division to reduce the frequency	F_{SYSCLK} = 64MHz	12.63	7.63	
			F_{SYSCLK} = 48MHz	9.92	6.17	
			F_{SYSCLK} = 36MHz	7.90	5.08	
			F_{SYSCLK} = 24MHz	5.75	3.98	
			F_{SYSCLK} = 16MHz	4.57	3.31	
			F_{SYSCLK} = 8MHz	2.82	2.23	
			F_{SYSCLK} = 4MHz	2.19	1.88	
			F_{SYSCLK} = 500KHz	1.61	1.58	

Note: 1. The above are the measured parameters;

2. When V_{DD} < 3V, the current power consumption will increase.

Table 3-7 Typical current consumption in Sleep mode, code with data processing running from internal flash memory or SRAM.

Symbol	Parameter	Condition		Typ.		Unit
				Enable all peripherals	Disable all peripherals	
I_{DD}(1)(2)	Supply current in Sleep mode (In this case, peripheral power supply and clock are maintained)	External clock	F_{SYSCLK} = 72MHz	10.98	5.33	mA
			F_{SYSCLK} = 48MHz	8.05	4.27	
			F_{SYSCLK} = 36MHz	6.87	4.06	
			F_{SYSCLK} = 24MHz	5.30	3.42	
			F_{SYSCLK} = 16MHz	4.34	3.08	
			F_{SYSCLK} = 8MHz	2.83	2.21	
			F_{SYSCLK} = 4MHz	2.37	2.06	
			F_{SYSCLK} =	1.97	1.93	

			500KHz			
		Runs in a high-speed internal RC oscillator (HSI), using AHB pre-division to reduce the frequency	F_{SYSCLK} = 64MHz	9.71	4.69	
			F_{SYSCLK} = 48MHz	7.73	3.96	
			F_{SYSCLK} = 36MHz	6.24	3.41	
			F_{SYSCLK} = 24MHz	4.76	2.87	
			F_{SYSCLK} = 16MHz	3.83	2.57	
			F_{SYSCLK} = 8MHz	2.47	1.84	
			F_{SYSCLK} = 4MHz	2.00	1.68	
			F_{SYSCLK} = 500KHz	1.59	1.55	

Note: 1. The above are the measured parameters;

2. When V_{DD} < 3V, the current power consumption will increase.

Table 3-8 Typical current consumption in Stop and Standby mode

Symbol	Parameter	Condition	Typ.	Unit
I_{DD}	Supply current in Stop mode	The voltage regulator is in Run mode, and both low- and high-speed internal RC oscillators and external oscillators are turned off (no independent watchdog)	455	uA
		The voltage regulator is in low power mode, and both low- and high-speed internal RC oscillators and external oscillators are turned off (no independent watchdog)	1.6	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog are on	2.8	
		The low-speed internal RC oscillator is on and the independent watchdog is off.	2.7	
		Low-speed internal RC oscillator and independent watchdog are off, low-speed external oscillator and RTC are off	1.6	
I_{DD_VBAT}	Supply current to the Backup domain (remove V_{DD} and	Low-speed external oscillator and RTC are on	2.4	

	V_{DDA}, use only V_{BAT} power)			

Note: The above are measured parameters.

3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSE_ext}	External clock frequency			8	25	MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage		$0.8V_{DD}$		V_{DD}	V
V_{HSEL}(1)	OSC_IN input pin low level voltage		0		$0.2V_{DD}$	V
$C_{in(HSE)}$	OSC_IN input capacitance			5		pF
$DuCy_{(HSE)}$	Duty Cycle			50		%

Note 1: Failure to meet this condition may cause a level recognition error.

Figure 3-3 Externally provided high frequency clock source circuit

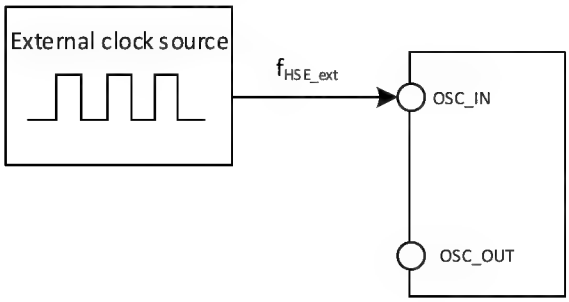


Table 3-10 From external low-speed clock

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSE_ext}	User external clock frequency			32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.8V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low voltage		0		$0.2V_{DD}$	V
$C_{in(LSE)}$	OSC32_IN input capacitance			5		pF
$DuCy_{(LSE)}$	Duty cycle			50		%

Figure 3-4 Externally provided low frequency clock source circuit

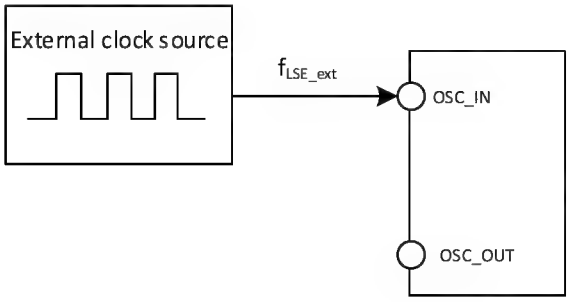


Table 3-11 High-Speed external clocks generated using one crystal/ceramic resonator

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{OSC_IN}	Resonator frequency		4	8	16	MHz
I_2(1)	HSE drive current	V_{DD} = 3.3V, 20p load		0.2		mA
g_m(1)	Oscillator transconductance	Startup		4.6		mA/V
$t_{SU(HSE)}$	Startup time	V_{DD} stabilization		1	2	ms

Note: 1. Design parameters

Circuit reference design and requirements:

The load capacitance of the crystal is generally 20pF (C_{L1}=C_{L2}, recommended 5~25pF). Please refer to the manufacturer's data manual of the crystal used.

Figure 3-5 Typical circuit for external 8M crystal

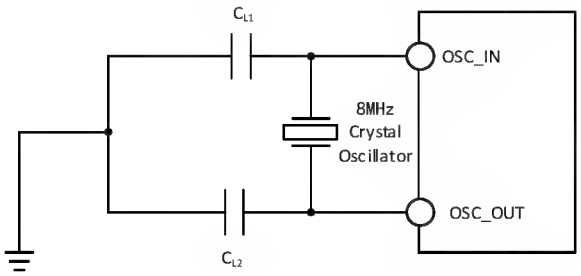


Table 3-12 Low-speed external clocks generated using a crystal/ceramic resonator (f_{LSE}=32.768KHz)

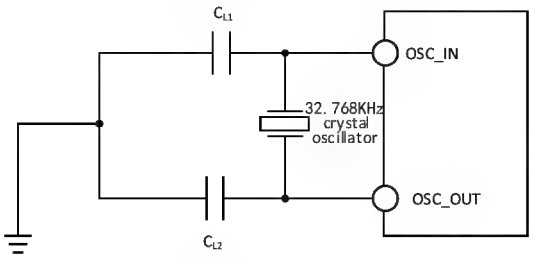
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_2(1)	LSE drive current	V_{DD} = 3.3V		0.5		uA
g_m(1)	Oscillator transconductance	Startup		13.5		uA/V
$t_{SU(LSE)}$	Startup time	V_{DD} stabilization		200	500	mS

Note: 1. Design parameters

Circuit reference design and requirements:

The load capacitance of the crystal generally does not exceed 15pF (C_{L1}=C_{L2}, recommended 5~15pF). In practice, please refer to the manufacturer's data manual of the crystal used.

Figure 3-6 Typical Circuit for External 32.768K Crystal



Note: The load capacitance CL is calculated by the following formula: CL = CL1 × CL2 / (CL1 + CL2) + Cstray, where C_{stray} is the capacitance of the pins and the capacitance associated with the PCB board or PCB, and its typical value is between 2pF and 7pF.

3.3.6 Internal Clock Source Characteristics

Table 3-13 Internal High-Speed (HSI) RC Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{HSI}	Frequency			8		MHz
$DuCy_{HSI}$	Duty cycle		45	50	55	%
ACC_{HSI}	Accuracy of HSI oscillator	T_A = 0°C~70°C	-1.8		1.8	%
		T_A = -40°C~85°C	-2.5		2.5	%
$t_{SU(HSI)}$	HSI oscillator startup stabilization time				8	us
$I_{DD(HSI)}$	HSI oscillator power consumption			200		uA

Table 3-14 Internal Low-Speed (LSI) RC Oscillator Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LSI}	Frequency		25	36	60	KHz
$DuCy_{LSI}$	Duty cycle		45	50	55	%
$t_{SU(LSI)}$	LSI oscillator startup stabilization time				82	us
$I_{DD(LSI)}$(1)	LSI oscillator power consumption			0.6		uA

Note: 1. Design parameters

3.3.7 PLL Characteristics

Table 3-15 PLL Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{PLL_IN}	PLL input clock		4	8	16	MHz
	PLL input clock duty cycle (1)		40		60	%
F_{PLL_OUT}	PLL multiplier output clock				80	MHz
t_{LOCK}(1)	PLL lock time				1000	$1/F_{PLL_IN}$

Note: 1. Design parameters

3.3.8 Wakeup Time from Low-power Mode

Table 3-16 Wakeup time from low-power mode

Symbol	Parameter	Condition	Typ.	Unit
$t_{wusleep}$	Wakeup from Sleep mode	Use HSI RC clock to wakeup	5.8	us
t_{wustop}	Wake up from Stop mode (voltage regulator is in Run mode)	HSI RC clock wakeup	253	us
	Wake up from the stop mode (voltage regulator is in low-power mode)	Time to wake regulator up from low-power mode + HSI RC clock wake-up + flash startup	253	us
$t_{WUSTDBY}$	Wake up from Standby mode	Time to wake regulator up from low-power mode + HSI RC clock wake-up + flash start	340	us

3.3.9 Memory Characteristics

Table 3-17 Flash memory characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{ERASE_128}	Page (256 bytes) programming time	T_A = -40°C~85°C	2.4	2.75	3.2	ms
t_{ERASE}	Page (256 bytes) erase time	T_A = -40°C~85°C	2.4	2.75	3.2	ms
t_{prog}	16-bit programming time	T_A = -40°C~85°C	2.4	2.75	3.2	ms
t_{ERASE}	Sector (1K bytes) erase time	T_A = -40°C~85°C	19	22	26	ms
t_{ME}	Mass erase time	T_A = -40°C~85°C	2.4	2.75	3.2	ms
V_{prog}	Programming voltage		2.7		5.5	V

Table 3-18 Flash memory endurance and data retention

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = 25°C	10K	80K(1)		次
t_{RET}	Data retention period		10			年

Note: The value of endurance is actually measured, not guaranteed.

3.3.10 I/O Port Characteristics

Table 3-19 General-purpose I/O static characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-level voltage	TTL port	-0.3		0.8	V
V_{IH}	Standard I/O pin, input high-level voltage	TTL port 2.7V<V_{DD}<4.2V	2		V_{DD}+0.3	V
		TTL port 4.2V≤V_{DD}<5.5V	0.55V_{DD}		V_{DD}+0.3	V
V_{IL}	Input low-level voltage	CMOS port	-0.3		0.8	V
V_{IH}	Input high-level voltage		0.65V_{DD}		V_{DD}+0.3	V
V_{hys}	Standard I/O pin Schmitt trigger voltage hysteresis			330		mV
I_{lkg}	Input leakage current				±1	uA
R_{PU}	Weak pull-up equivalent group		30	42	55	KΩ
R_{PD}	Weak pull-down equivalent group		30	42	55	KΩ
C_{IO}	I/O pin capacitor			5		pF

Note: The above are guaranteed design parameters.

Output Drive Current Characteristics

The GPIOs (General-purpose Input/Output Ports) can absorb or output up to ±8mA of current and absorb or output ±20mA of current (not strictly up to V_{OL}/V_{OH}). In user applications, the total current driven by all IO pins must not exceed the absolute maximum ratings given in section 3.2:

Table 3-20 Output voltage characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{OL}	Output low level, single pin absorbs current	TTL port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, single pin output current		V_{DD}-0.4		V
V_{OL}	Output low level, single pin absorbs current	CMOS port, I_{IO} = +8mA 2.7V< V_{DD} <5.5V		0.4	V
V_{OH}	Output high level, single pin output current		2.3		V
V_{OL}	Output low level, single pin absorbs current	I_{IO} = +20mA 2.7V< V_{DD} <5.5V		1.3	V
V_{OH}	Output high level, single pin output current		V_{DD}-1.3		V

Note: If more than one IO pin is driven at the same time in the above conditions, the sum of the currents must not exceed the absolute maximum ratings given in section 3.2. Also when multiple IO pins are driven at the same time, the high current at the power/ground point can cause a voltage drop that prevents the voltage of the internal IOs from reaching the supply voltage in the table, which results in a drive current that is less than the nominal value.

Table 3-21 Input/Output AC Characteristics

MODEx[1:0] configuration	Symbol	Parameter	Condition	Min.	Max.	Unit
10 (2MHz)	$F_{max(IO)out}$	Maximum Frequency	CL=50pF, V_{DD}=2.7-5.5V		2	MHz
	$t_{f(IO)out}$	Output high-to-low level fall time	CL=50pF, V_{DD}=2.7-5.5V		125	ns
	$t_{r(IO)out}$	Output low-to-high rise time			125	ns
01 (10MHz)	$F_{max(IO)out}$	Maximum Frequency	CL=50pF, V_{DD}=2.7-5.5V		10	MHz
	$t_{f(IO)out}$	Output high-to-low level fall time	CL=50pF, V_{DD}=2.7-5.5V		25	ns
	$t_{r(IO)out}$	Output low-to-high rise time			25	ns
11 (50MHz)	$F_{max(IO)out}$	Maximum Frequency	CL=30pF, V_{DD}=2.7-5.5V		50	MHz
			CL=50pF, V_{DD}=2.7-5.5V		30	MHz
	$t_{f(IO)out}$	Output low-to-high rise time Maximum Frequency	CL=30pF, V_{DD}=2.7-5.5V		20	ns
			CL=50pF, V_{DD}=2.7-5.5V		5	ns
	$t_{r(IO)out}$	Output high-to-low level fall time	CL=30pF, V_{DD}=2.7-5.5V		8	ns
			CL=50pF, V_{DD}=2.7-5.5V		12	ns
	t_{EXTIpw}	EXTI controller detects the pulse width of the external signal		10		ns

Note: All of the above are guaranteed by design parameters.

3.3.11 NRST Pin Characteristics

Table 3-22 External reset pin characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage		-0.3		0.8	V
$V_{IH(NRST)}$(1)	NRST input high level voltage		0.65V_{DD}		V_{DD}+0.5	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			330		mV
R_{PU}(2)	Weak pull-up equivalent resistance		30	42	55	KΩ
$T_{F(NRST)}$(1)	NRST input can be filtered for pulse width				4	ns
$T_{NF(NRST)}$(1)	NRST input cannot be filtered pulse width		20			ns

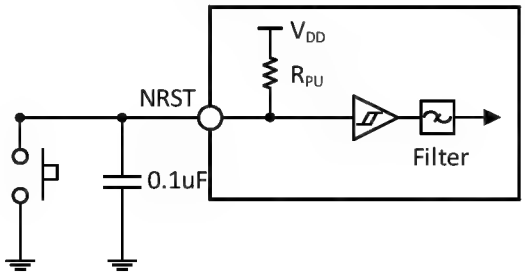
Note:

1. Design parameters;

2. The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (about 10%).

Circuit reference design and requirements:

Figure 3-7 Typical circuit of external reset pin



3.3.12 TIM Timer Characteristics

Table 3-23 TIMx characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
$t_{res(TIM)}$	Timer reference clock		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	13.9		ns
F_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$ = 72MHz	0	36	MHz
R_{esTIM}	Timer resolution			16	位
$t_{COUNTER}$	16-bit counter clock cycle when the internal clock is selected		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz	0.0139	910	us
t_{MAX_COUNT}	Maximum possible count			65535	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72MHz		59.6	s

Note: All of the above are guaranteed by design parameters.

3.3.13 I2C Interface Characteristics

Figure 3-8 I2C bus timing diagram

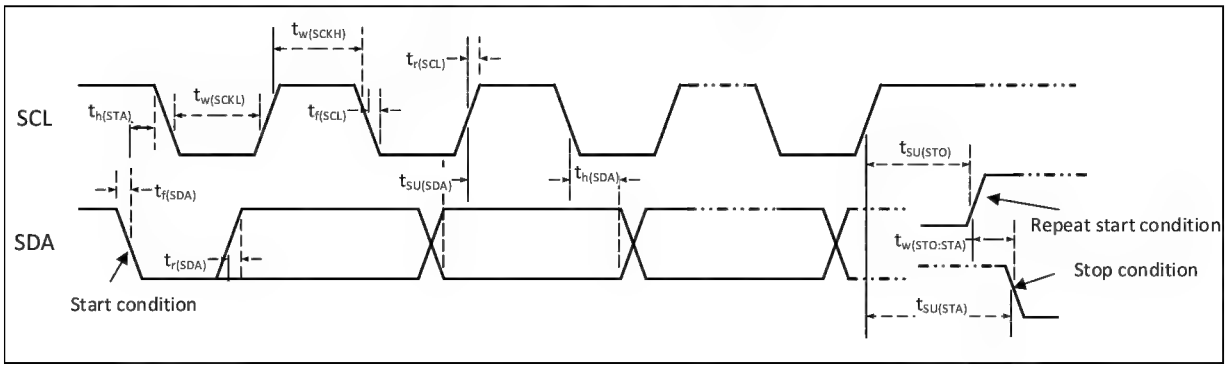


Table 3-24 I2C interface characteristics

Symbol	Parameter	Standard I2C		Fast I2C		Unit
		Min.	Max.	Min.	Max.	
$t_{w(SCKL)}$	SCL clock low level time	4.7		1.2		us
$t_{w(SCKH)}$	SCL clock high level time	4.0		0.6		us
$t_{SU(SDA)}$	SDA data setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0		0	900	ns
$t_{r(SDA)}/t_{r(SCL)}$	SDA and SCL rise time		1000	20		ns
$t_{f(SDA)}/t_{f(SCL)}$	SDA and SCL fall time		300			ns
$t_{h(STA)}$	Start condition hold time	4.0		0.6		us
$t_{SU(STA)}$	Repeated start condition setup time	4.7		0.6		us
$t_{SU(STO)}$	Stop condition setup time	4.0		0.6		us
$t_{w(STO:STA)}$	Time from stop condition to start condition (bus free)	4.7		1.2		us
C_b	Capacitive load for each bus		400		400	pF

3.3.14 SPI Interface Characteristics

Figure 3-9 SPI timing diagram in Master mode

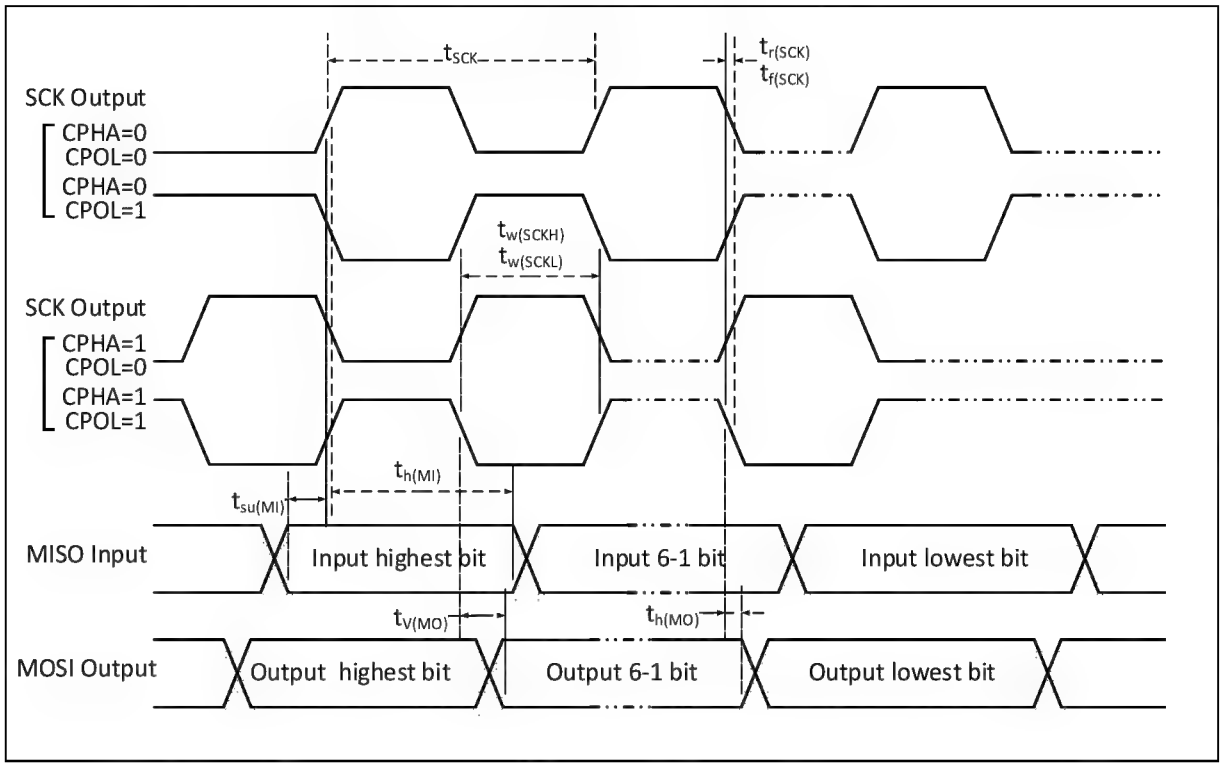


Figure 3-10 SPI timing diagram in Slave mode (CPHA=0)

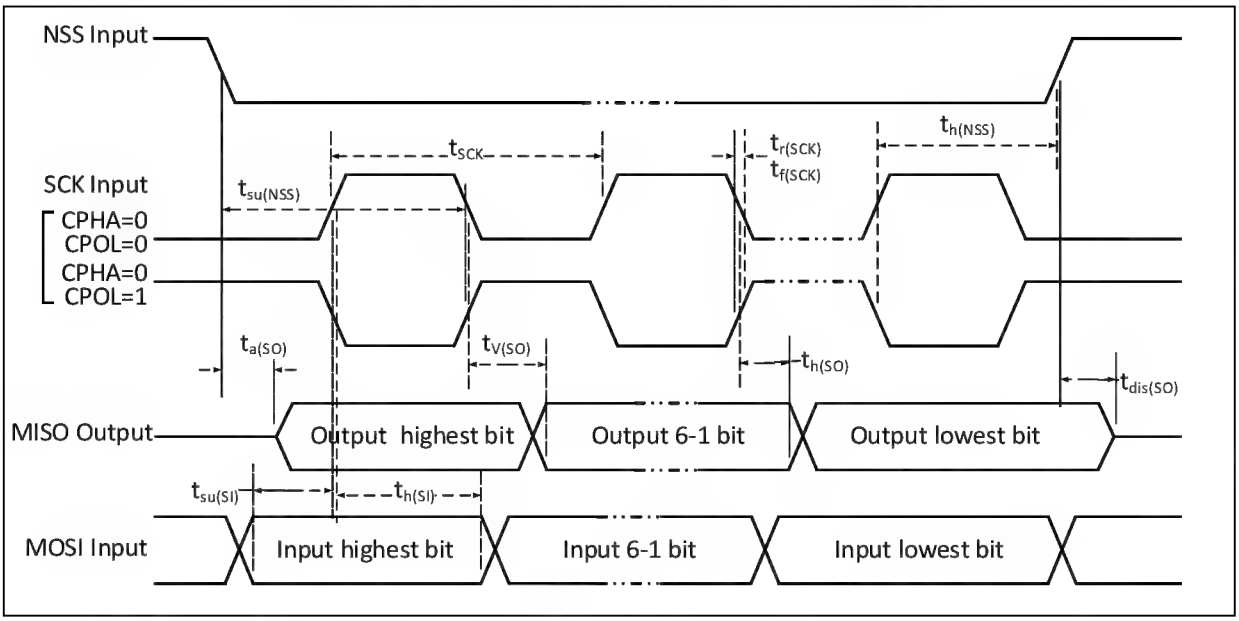


Figure 3-11 SPI timing diagram in Slave mode (CPHA=1)

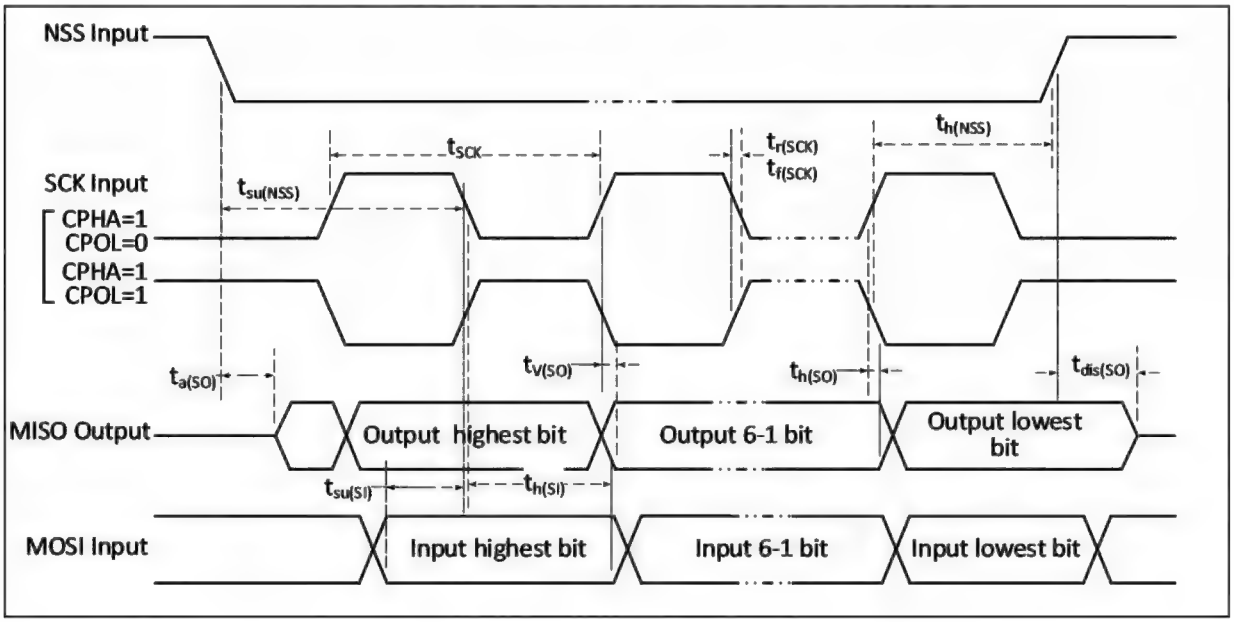


Table 3-25 SPI interface characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
f_{SCK}/t_{SCK}	SPI clock frequency	Master mode		36	MHz
		Slave mode		36	MHz
$t_{r(SCK)}/t_{f(SCK)}$	SPI clock rise and fall time	Load capacitance: C = 30pF		20	ns
$t_{SU(NSS)}$	NSS setup time	Slave mode	$2t_{HCLK}$		ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$		ns
$t_{w(SCKH)}/t_{w(SCKL)}$	SCK high-level and low-level time	Master mode, f_{PCLK} = 36MHz, Prescaler factor = 4	40	60	ns
$t_{SU(MI)}$	Data input setup time	Master mode	5		ns
$t_{SU(SI)}$		Slave mode	5		ns
$t_{h(MI)}$	Data input hold time	Master mode	5		ns
$t_{h(SI)}$		Slave mode	4		ns
$t_{a(SO)}$	Data output access time	Slave mode, f_{PCLK} = 20MHz	0	$1t_{HCLK}$	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	0	10	ns
$t_{V(SO)}$	Data output valid time	Slave mode (After enable edge)		25	ns
$t_{V(MO)}$		Master mode (After enable edge)		5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (After enable edge)	15		ns
$t_{h(MO)}$		Master mode (After enable edge)	0		ns

3.3.15 USB Interface Characteristics

Table 3-26 USB interface I/O characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{DD}	USB operating voltage	Not enable USB5VSEL control bit	3.0	3.6	V
		Enable USB5VSEL control bit	4.2	5.5	

V_{SE}(1)	USB operating voltage	V_{DD} = 3.3V	1.2	1.9	V
		V_{DD} = 5V	1.2	2	
V_{OL}	Static output low level			0.3	V
V_{OH}	Static output high level		2.8	3.6	V

Note: 1. Design parameters;

3.3.16 12-bit ADC Characteristics

Table 3-27 ADC characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDA}	Supply voltage		3.0		5.5	V
f_{ADC}	ADC clock frequency				14	MHz
f_S	Sampling rate				1	MHz
f_{TRIG}	External trigger frequency	f_{ADC} = 14MHz			875	KHz
					16	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_{AIN}	External input impedance				58	KΩ
R_{ADC}	Sampling switch resistance			0.6	1.3	KΩ
C_{ADC}	Internal sample and hold capacitor			30		pF
t_{lat}	Injected trigger conversion latency	f_{ADC} = 14MHz			0.143	us
					2	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 14MHz			0.143	us
					2	$1/f_{ADC}$
t_s	Sampling time	f_{ADC} = 14MHz	0.107		17.1	us
			1.5		239.5	$1/f_{ADC}$
t_{STAB}	Power-on time				1	us
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 14MHz	1		18	us
			14		252	$1/f_{ADC}$

Note: The above are guaranteed design parameters.

Formula: Maximum R_{AIN}

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. where N=12 (indicating 12-bit resolution).

Table 3-28 Maximum R_{AIN} at f_{ADC} = 14MHz

T_S (cycle)	t_S (us)	Maximum R_{AIN}(kΩ)
1.5	0.11	0 (Not recommended)
7.5	0.54	1.1
13.5	0.96	2.6
28.5	2.04	6.2

41.5	2.96	9.4
55.5	3.96	12.9
71.5	5.11	16.8
239.5	17.1	58

Note: The above are guaranteed design parameters.

Cp indicates the parasitic capacitance on the PCB and pads (about 5pF), which may be related to the quality of the pads and PCB layout. Larger values of Cp will reduce the conversion accuracy and the solution is to reduce the f_{ADC} value.

Figure 3-12 ADC typical connection diagram

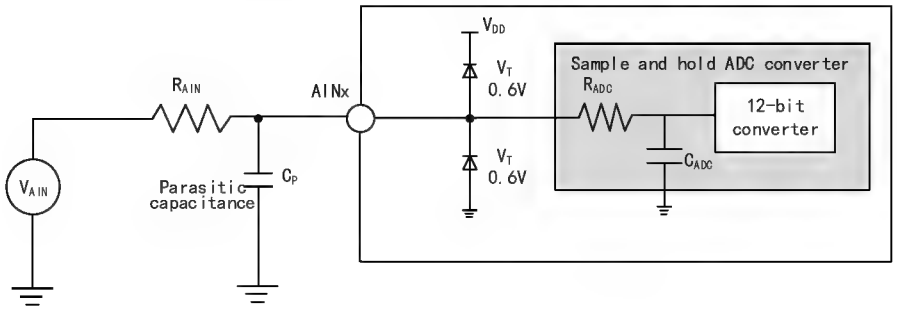
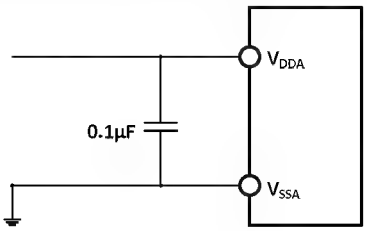


Figure 3-13 Analog power supply and decoupling circuit reference



3.3.17 TS Characteristics

Table 3-29 TS characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Avg_Slope	Average slope		3.3	4.3	5.3	mV/°C
V_{25}	Voltage at 25°C		1.1	1.34	1.6	V
T_{S_temp}	ADC sampling time when reading temperature	f_{ADC} = 14MHz			17.1	us

Note: The above are guaranteed design parameters.

3.3.18 Touch-key Characteristics

Table 3-30 Touch-key characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{TKey}	Module operating mode	V_{DD}=3.3V	211	270	421	uA

Chapter 4 Package and Ordering Information

Packages

Order model	Package form	Body size	Pin pitch	Package description	Packing type
CH32V103R8T6	LQFP64M	10*10mm	0.5mm	Low Profile Quad Flat Pack	Tray
CH32V103C6T6	LQFP48	7*7mm	0.5mm	Low Profile Quad Flat Pack	Tray
CH32V103C8T6	LQFP48	7*7mm	0.5mm	Low Profile Quad Flat Pack	Tray
CH32V103C8U6	QFN48×7	7*7mm	0.5mm	Quad Flat No-Lead Package	Tray

Note: 1. The packing type of QFP/QFN is usually tray.

*2. Size of tray: The size of Tray is generally a uniform size (322.6*135.9*7.62). There are differences in the size of the restriction holes for different package types, and there are differences between different packaging factories for tubes, please confirm with the manufacturer for details.*

Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.

Figure 4-1 LQFP64M package

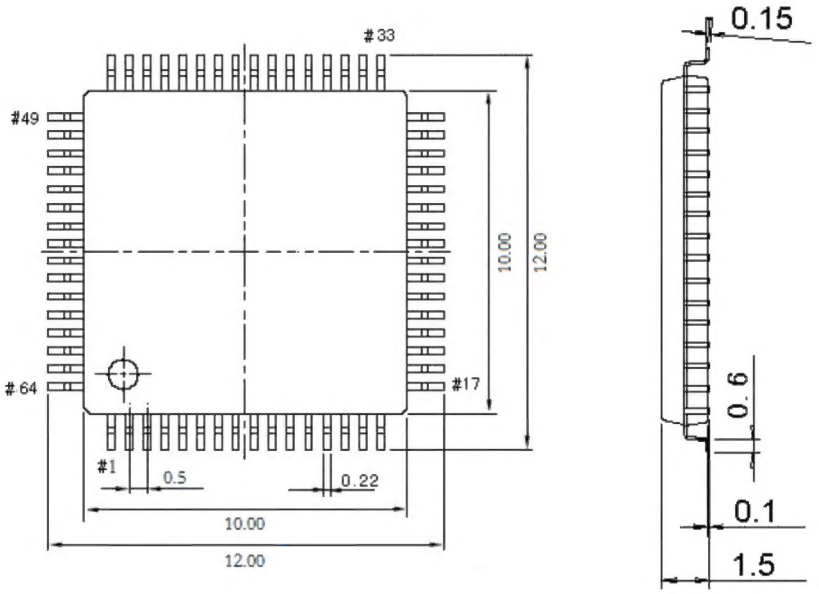


Figure 4-2 LQFP48 package

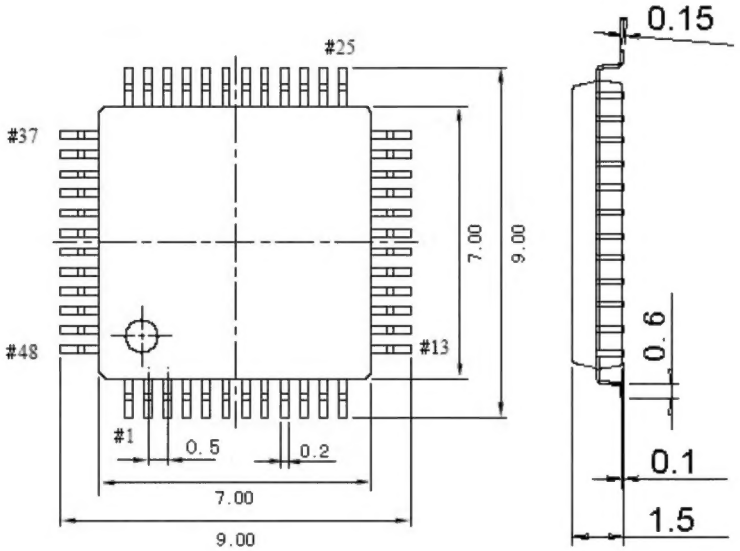
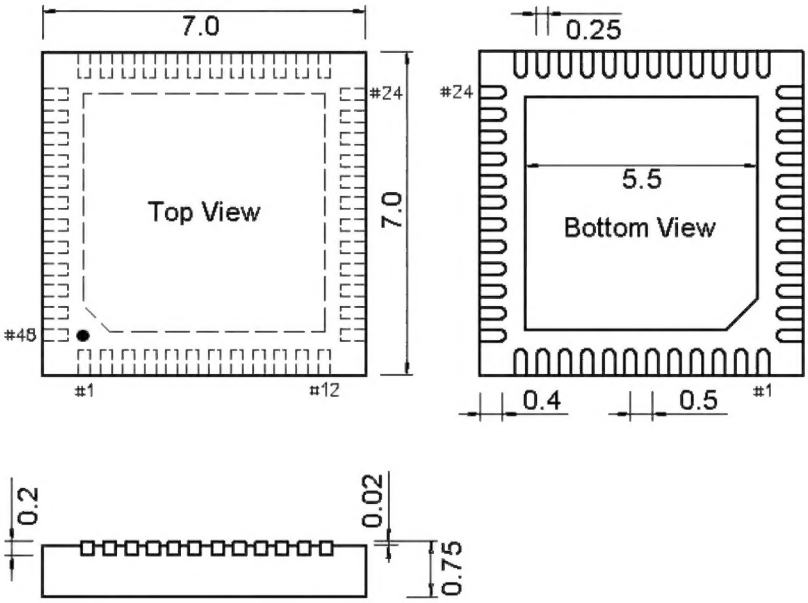


Figure 4-3 QFN48×7 package



Series Product Naming Rules

Example: CH32 V 3 03 R 8 T 6

Device family

F = ARM-based, general-purpose MCU
V = QingKe RISC-V-based, general-purpose MCU
L = QingKe RISC-V-based, low power MCU
X = QingKe RISC-V-based, Dedicated architecture or special IO

Product type

0 = QingKe V2/V4 core, great value version, clock frequency<=48M
1 = M3 / QingKe V3/V4 core, basic version, clock frequency<=72M
2 = M3 / QingKe V4 non-floating-point core, enhanced version, clock frequency<=144M
3 = QingKe V4F floating-point core, clock frequency<=144M

Device subfamily

03 = General-purpose
05 = Connectivity (USB high-speed, SDIO, CAN)
07 = Interconnectivity (USB high-speed, CAN, Ethernet, DVP, SDIO, FSMC)
08 = Wireless (BLE5.X, CAN, USB, Ethernet)
35 = Connectivity (USB, USB PD/Type C)
33 = Connectivity (USB)

Pin count

J = 8 pins A = 16 pins F = 20 pins G = 28 pins
K = 32 pins T = 36 pins C = 48 pins R = 64 pins
W = 68 pins V = 100 pins Z = 144 pins

Flash memory size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory
7 = 48 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

Temperature range

6 = -40°C~85°C (Industrial-grade)
7 = -40°C~105°C (Automotive-grade 2)

3 = -40℃~125℃ (Automotive-grade 1)

D = -40℃~150℃ (Automotive-grade 0)